

Code: IT3T1

**II B.Tech - I Semester–Regular/Supplementary Examinations  
November 2017**

**DIGITAL SYSTEM DESIGN  
(INFORMATION TECHNOLOGY)**

Duration: 3 hours

Max. Marks: 70

**PART – A**

Answer *all* the questions. All questions carry equal marks

11x 2 = 22 M

1.

a) Determine the base for the following operators.

i)  $(44 + 24)_b = (73)_{10}$

ii)  $(101 + 10)_b = (25)_8$

b) Convert the following numbers into base 4

i)  $(70)_8$

ii)  $(FFA)_{16}$

c) Represent the decimal digit 9 in Excess-3 code and 8 4 -2 -1 code.

d) Simplify the following logic expressions.

$$(A + B)(\bar{A} + C)(B + \bar{C})$$

e) Obtain complement for the given expression

$$(A + B)\bar{C}D + EF$$

f) Simplify the following expressions using truth table

$$\overline{A \oplus B} \oplus \overline{AB}$$

g) A three variable logic function f (A,B,C) is implemented with 4 to 1 Multiplexer such that data lines are used for variable A and select lines are for B, C variables if

$$X_0 = X_3 = H, X_1 = \bar{A} \& X_2 = A \text{ obtain minterm list.}$$

- h) Draw full adder circuit using 2 half adders and 1 OR gate.
- i) Implement the following function using NAND gates  
 $D(\bar{A} + \bar{C})ED$
- j) The first half adder sum and carry are used as inputs of second half adder. What are the logic expressions of sum and carry outputs of second half adder. Assume A, B are inputs of first half adder.
- k) Give the truth table of negative edge triggered J-K Flipflop with active high clear input.

### PART – B

Answer any **THREE** questions. All questions carry equal marks.

3 x 16 = 48 M

2. a) Convert given hexadecimal number **7DF** to Base 4 number and base 8 number. **4 M**

b) Perform the following operation using 2's complement form. Assume 8 bit word length including sign bit.

$(-32) + (-27)$  **8 M**

c) Convert the following number to base 2 and hence obtain its 2's complement.  $(233233)_4$  **4 M**

3. a) Simplify the following logic expression

$Y = AB + \bar{A}C + \bar{B}D + \bar{C}D + C\bar{D}$  **4 M**

- b) Obtain minimal SOP expression using K-Map and hence draw the circuit using 2 input NAND gates. 12 M

$$f(A, B, C, D) = \sum 0,1,2,4,6,9,10 + d (3,11,12,13,15)$$

4. a) Implement the following logic functions with 8 to 1 multiplexer. 8 M

$$f(A, B, C, D) = \sum 0,3,6,8,11,13,15$$

- b) Implement the following function using 3 to 8 line De-multiplexer and 2 OR gates. 8 M

$$f_1(A, B, C) = \bar{A}B + A\bar{B} + \bar{B}\bar{C}$$

$$f_2(A, B, C) = (\bar{A} + \bar{C})(\bar{B} + \bar{C})(\bar{A} + \bar{B})$$

5. Prepare PLA programming table and hence implement the following functions using minimum number of AND gates and OR gates of PLA 16 M

$$f_1(A, B, C, D) = \sum 0,3,4,5,6,7,8,11,12,15$$

$$f_2(A, B, C, D) = \sum 1,2,4,5,6,7,9,10,13,14$$

$$f_3(A, B, C, D) = \sum 1,4,5,6,7,8,9,10,11,13$$

6. Draw the state diagrams of MOD 6 UP/DOWN Counter and hence design synchronous circuit using T-Flipflops with active low clear terminal. 16 M